## REMARKS

1. In the above captioned office action, the Examiner rejected claims 1, 3-11, 23-25, and 27-32 under 35 USC § 112, second paragraph; and claims 1, 3-9, 27, 28, 30 and 31 under 35 USC § 103 as being unpatentable over Bruce et al. (US Patent No. 4,344,133) in view of Johnson et al. (US Patent No. 4,420,806). These rejections have been traversed and reconsideration is hereby respectfully requested.

2. The applicants have amended the claims and, as such, only claims 1, 3 - 10, 23 and 27 remain. Thus, only these claims will be discussed in view of the Examiner's rejections.

3. Claims 1, 3 - 10, 23 and 27 have been rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particular point out and distinctly claim the subject matter which the applicants regard as the invention. Given the degree of changes to the claims, the applicants believe that each of the remaining claims overcome this rejection.

4. Claims 1, 3-9 and 27 have been rejected under 35 USC § 103 as being unpatentable over Bruce et al. in view of Johnson et al. As amended, claim 1 claims an interrupt mask disable circuit that includes first and second logic circuitry. The first logic circuitry provides an interrupt signal when the interrupt is requested and a mask signal is disabled. The mask signal is generated by the second logic circuitry which receives a mask activation signal and a mask override signal. If the mask override signal is active, regardless of the state of the mask activation signal, the mask signal will be disabled, thus allowing the first logic circuitry to pass the interrupt signal to a processor.

In contrast, Bruce et al. teaches a method for synchronizing software and hardware. In general, the method involves providing a SYNC instruction to a processor which stops the processor from executing instructions. The processor restarts only when an interrupt line is

activated. (See column 3, lines 56 - 65.) The circuitry that performs this function is shown in Fig. 2 and functionally described with reference to Fig. 3. As described with reference to Fig. 3 (column 7, line 59 through column 8, line 45), Bruce teaches a method that begins when a sync instruction is received. The sync instruction sets a sync latch and stops the processor from further instruction execution. When an interrupt is received, the latch is reset and if the interrupt is masked, the processor resumes program execution at the placed it stopped when the sync instruction was received. If the interrupt is not masked, the processor jumps to program instructions identified by a vector.

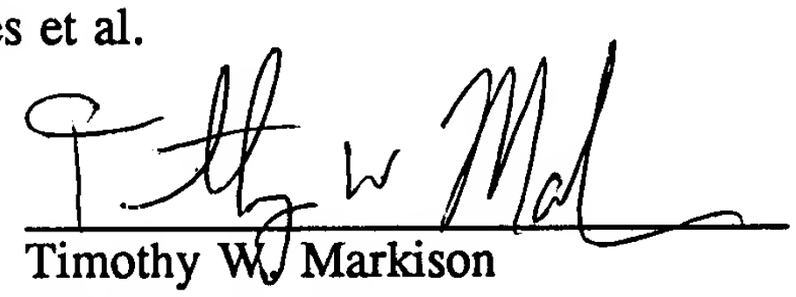
Johnson et al. teaches an interrupt matrix for use in a multiprocessor network. The matrix stores the current status of processor interrupts based on the originating processor and the destination processor. The contents of the matrix can be selectively masked and prioritized by the destination processor. (See column 1, line 62 - column 2, line 30.) The processor enables mask logic via line 21 when an interrupt request is received via line 20 and provides a interrupt vector via line 19. (See column 4, lines 37 - 39.)

As discussed, Bruce et al. and Johnson et al. teach masking an interrupt via a mask signal. However, neither reference teaches or suggests overriding the mask signal as is claimed in the present invention. Such an override can be initiated by a hardware condition, such as the processor being in an idle state. In this state, a restart interrupt should not be masked, such that the processor can be restarted without having to reboot the system.

Bruce et al. and Johnson et al. teach enabling a mask signal when an interrupt is to be ignored and not enabling the mask signal when the interrupt is to be performed. Thus, if a restart interrupt were masked in a system incorporating the teachings of Bruce et al. and Johnson et al., the processor would not be able to restart after an idle condition without a system reboot. Thus, the applicants believe that claims 1, 3 - 10, and 27 are not obvious in view of Bruce and Johnson and, as such, are in condition for allowance.

5. The Examiner is invited to contact the undersigned by telephone or facsimile if the Examiner believes that such a communication would advance the prosecution of the present application.

RESPECTFULLY SUBMITTED,
Bowles et al.

By: 
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